

(19)



JAPANESE PATENT OFFICE

## PATENT ABSTRACTS OF JAPAN

(11) Publication number: **05013665 A**(43) Date of publication of application: **22.01.93**

(51) Int. Cl. **H01L 25/065**  
**H01L 25/07**  
**H01L 25/18**  
**H01L 21/60**  
**H05K 1/18**

(21) Application number: **03183498**(71) Applicant: **NEC CORP**(22) Date of filing: **28.06.91**

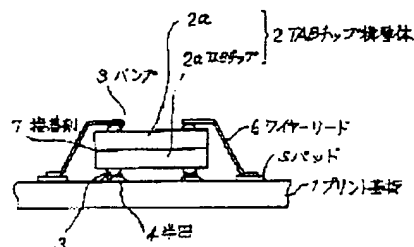
(72) Inventor: **YAMAUCHI FUSHIMI**  
**KAWAZUMI MASARU**

(54) **METHOD FOR MOUNTING TAB CHIP**

## (57) Abstract:

**PURPOSE:** To increase a mounting rate of TAB chips on a printed board by piling up at least two TAB chips and then by mounting these chips on the printed board.

**CONSTITUTION:** At least two TAB chips 2a, 2a are joined with an adhesive 7 with end faces having no bump 3 faced each other. The bumps 3 are located on an upper and a lower end face of the TAB chip laminated body 2 and then the TAB chip laminated bodies 2 are piled up. Next, the bumps 3 of the lower TAB chip 2a are joined with a printed board 1 with solder 4. Meanwhile, the bumps 3 of the upper TAB chip 2 are connected with one end of wire leads 6 and the other end of the wire leads is joined to a pad of the printed board 1. By this method, a mounting rate on the printed board 1 can be increased and a TAB chip mounting area can be reduced substantially.



COPYRIGHT: (C)1993,JPO&amp;Japio